REMARKS

KAMVYSSELIS

The present disclosure is directed to the problem of copying data that spans at least two slots. In such cases, it is may not be possible to tell whether the data is valid until all slots have been filled.

A difficulty arises in the prior art because each time one writes to a slot, one queues a mirroring request for that slot. There is no guarantee, in such cases, that a mirror request for a slot will be executed only when *all* the data (which may span several slots) has been copied. Therefore, in prior art systems, it is quite possible for data to be copied to a mirror site *before* the validity of that data can be checked.

Kamvysselis[1] is an example of one such prior art system. In *Kamvysselis*, copying data to a slot triggers the queuing of a corresponding mirror request. If, after another slot has been filled, one determines that the data in the first slot was invalid all along, there is little that can be done about it. The first mirror request for that first slot would already have been queued for execution.

The invention recited in claim 1 is directed at *avoiding* the foregoing difficulty associated with data that spans multiple slots. *Kamvysselis* does not discuss data spanning multiple slots. Not surprisingly, *Kamvysselis* does not teach ways to prevent the foregoing difficulty.

SECTION 102 REJECTION OF CLAIMS 2, 7, 9, 15 AND PROGENY

***Kamvysselis* fails to teach deleting mirror requests in response to invalid data**

As best understood, the Examiner regards claim 1's step of

> "if the data written to the temporary storage location is invalid, deleting the mirror requests"

to be met by *Kamvysselis*' step **124** in FIG. 6.

---

[1] *Kamvysselis*, U.S. Patent No. 6,496,908.

However, a careful review of the flow chart in FIG. 6 will reveal that step **124** is only executed when data is *valid*. Step **124** is *not* executed when data is *invalid*.

The Examiner suggests that the determination of whether data is valid occurs at step **106**.

It is apparent from inspection of FIG. 6 that if data is invalid, control follows the "NO" branch to the left of the figure. This branch leads to steps **100** and **102**. It is also apparent from inspection of FIG. 6 that step **124** cannot be executed if one follows the "NO" branch at step **106**. Step **124** can only be carried out if data is valid, i.e. if one follows the "YES" branch in FIG. 6.

Construing "*the* data"

In construing the claims, it is useful to maintain strict consistency in what is regarded as being "the data" defined in the preamble.

As is apparent from the first paragraph of claim 2, "the data" is clearly intended to span multiple slots. A "first portion" of "*the* data" is stored in one slot, while a "second portion" of "*the* data" is stored in another slot. Thus, it is important not to construe what is in the first slot as "*the* data" recited in the preamble. While the content of the first slot is indeed "data," it is not "*the* data" referred to in the preamble. It is only a "first portion of *the* data."

***Kamvysselis* fails to teach writing portions of data to respective slots**

Claim 2 includes the limitation:

> "writing first and second portions of the data to respective first and second slots within a temporary storage location"

The Examiner identifies two passages as allegedly disclosing this limitation: col. 1, lines 49-56 and col. 3, lines 31-44.

The first passage[2] describes mirroring source data at two or more mirrors. This results in *the same data* being copied to two different data storage systems, not to "writing first and second

[2] *Kamvysselis*, col. 1, lines 49-56.

portions of '*the* data' to respective first and second slots." What this first passage describes is copying *all* of the data, and not just a first portion thereof, to *both* mirroring systems.

In other words, if "*the* data" is "ABCD," then the cited passage teaches copying *the* data "ABCD," to both mirror-1 and mirror-2. As a result, both mirror-1 and mirror-2 contain "ABCD." This is plainly inconsistent with "writing first and second *portions* of '*the* data' to respective first and second slots." *Kamvysselis* does not disclose, for example, writing a first portion, such as "AB," to mirror-1, and a second portion, such as "CD," to mirror-2.

Moreover, the act of copying to two distinct mirroring systems can hardly be viewed as copying to two different slots "within a temporary storage location." The mirroring systems of *Kamvysselis* are distinct from each other. It is not the case that the two mirroring system are somehow "within" a temporary storage location.

The second passage[3] describes how a host adaptor periodically de-stages data from a temporary storage location **24** to a disk **18**. It is unclear what the Examiner has in mind as being "first and second portions of the data" in this case. The passage, after all, only discusses "data" without suggesting that this data is to somehow be divided into "first and second portions."

Moreover, since the second passage refers to only one data storage location **24**, it is also unclear what the Examiner has in mind as being "first and second slots."

***Kamvysselis* fails to teach deleting plural mirror requests**

Claim 2 recites the additional limitation

"deleting the mirror requests"

As best understood, the Examiner regards the step of "deleting the mirror requests" as being disclosed by step **124** of FIG. 6. However, step **124** refers to deleting a *single* mirror request. It

[3] *Kamvysselis*, col. 3, lines 31-44.

does not refer to deleting *plural* mirror requests. Nor is there any suggestion of deleting plural mirror requests since FIG. 6 only refers to a single mirror request.

***Kamvysselis* fails to teach buffering mirror requests**

Claim 2 recites

> "buffering a first mirror request to copy the first portion from the first temporary storage location to a mirror"

As best understood, the Examiner regards the queuing of a mirror request to correspond to buffering a mirror request **42a-d** in a mirror queue **40a**.

However, "buffering" and "queuing" are different. In fact, buffering a mirror request need not involve the mirror queue at all. It is the step of queuing the mirror request for execution that involves the mirror queue.

The introduction of a buffering step enables mirror requests to be generated but withheld from a mirror queue until such time as those mirror requests are known to correspond to valid data. Once this occurs, the mirror requests are all released to the mirror queue together. If the data is invalid, *all* the mirror requests are deleted. This procedure avoids the problem of having released a mirror request to the queue only to discover later that the data being mirrored by that request is invalid.

The fact that the mirror request is placed in a queue, and that some time may elapse before mirroring actually occurs, is not definitive of buffering. By way of analogy, a stream of machine gun bullets in-flight is in effect a "queue" of bullets waiting to reach their target. However, nobody would seriously say that these bullets are somehow "buffered" because they have not yet reached their target.

The Examiner also cites text that refers to the request buffers **44.** However, a request buffer **44** is not a mirror request **42**. Nor does a request buffer **44** in any way buffer mirror requests **42**. A request buffer **44** contains information for keeping track of which mirror requests

42 have been executed, and which await execution in a queue **40**. The request buffer **44** also includes information about what is to be mirrored. Accordingly, the request buffer **44** is irrelevant to claim 2's limitation of "buffering a first mirror request."

Claims 3-6 all depend on claim 2 and are allowable for at least the same reason.

Claims 7, 8, and 9 recite limitations similar to claim 2 and are allowable for at least the same reasons.

Claims 15 and its dependent claims 16-19 include limitations similar to claims 2-6 and are therefore patentable for at least the same reasons.

SECTION 103 REJECTION OF CLAIMS 10-13

The Examiner rejects claims 10-13 as being rendered obvious by the combination of *Kamvysselis* and *Lecrone*.[4]

Lecrone was filed on October 30, 2002 and issued on October 11, 2005. The present application has a priority date of June 29, 2003, which is before *Lecrone*'s issue date but after its filing date. Accordingly, *Lecrone* is available as prior art only under 35 USC 102(*e*).

At the time the invention was made, both the claimed invention and *Lecrone* were assigned to or under obligation to assign to a common assignee. Accordingly, under 35 USC 103(*c*)(1), *Lecrone* is not available for use in making an obviousness rejection.

SECTION 102 REJECTION OF CLAIMS 10-13

The Examiner refers to a section 102 rejection of claims 10-13 based on *Kamvysselis*. However, the Examiner also states that "*Kamvysselis* fails to teach a holding pen"[5] and that it was this lack of a holding pen in *Kamvysselis* that required the inclusion of *Lecrone*.

---

[4] *Lecrone*, U.S. Patent No. 6,954,835.
[5] *Office Action*, page 5.

Based on the foregoing remarks, Applicant suspects that claims 10-13 were mistakenly included in the listing of claims on page 4 of the office action and that no such rejection is intended.

SECTION 102 REJECTION OF CLAIMS 6 AND 19

Claim 6 recites the additional of limitation of

> "buffering the mirror request in a memory location separate from the temporary storage location."

Based on the cited text, the Examiner appears to regard one mirror queue **40a** as a "temporary storage location" and another mirror queue **40b** as "a memory location separate from the temporary storage location (i.e., the other mirror queue **40a**)."

However, according to the first limitation of claim 2:

> "writing first and second portions of the data to respective first and second slots within a temporary storage location,"

there must be "first and second slots within a temporary storage location." It is quite clear in FIG. 1 that the slots **24** are not at all "within" the mirror queues **40a-d**. Therefore, a mirror queue **40** fails to satisfy this requirement. Accordingly, a mirror queue **40** cannot properly be regarded as a "temporary storage location."

SUMMARY

Now pending in this application are claims 2-19, with claims 2, 7-10, and 15 being independent.

Applicant has advanced only selected arguments, and has done so only for selected claims. This is not, however, to be construed as an admission that no other grounds for patentability of the claims exist.

No additional fees are believed to be due in connection with the filing of this response. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: August 10, 2006

Faustino A. Lichauco
Reg. No. 41,942

Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

21395987.doc